PERICOM®

PI49FCT805T
PI49FCT2805T

Fast CMOS Clock Driver/Buffer

Features

- Extremely low output skew: 0.5ns
- Monitor output pin
- Clock busing with Hi-Z state control
- TTL input and CMOS output compatible
- Extremely low static power (1mW, typ.)
- Hysteresis on all inputs
- Device models available on request
- Industrial Operation at -40ºC to +85ºC
- Packaging (Pb-free & Green available):

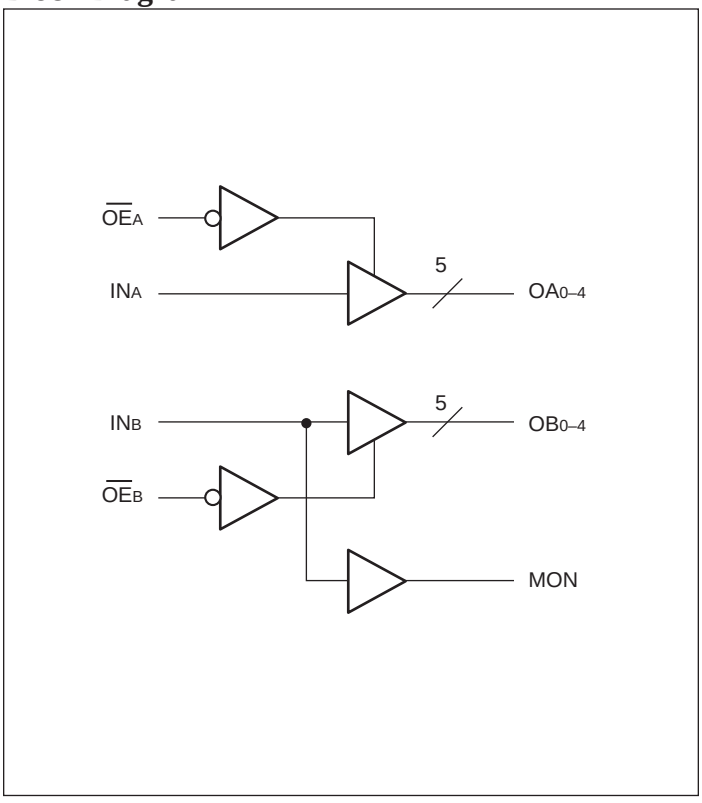
– 20-pin 209-mil wide SSOP (H)
– 20-pin 300-mil wide SOIC (S)
– 20-pin 150-mil wide QSOP (Q)

Description

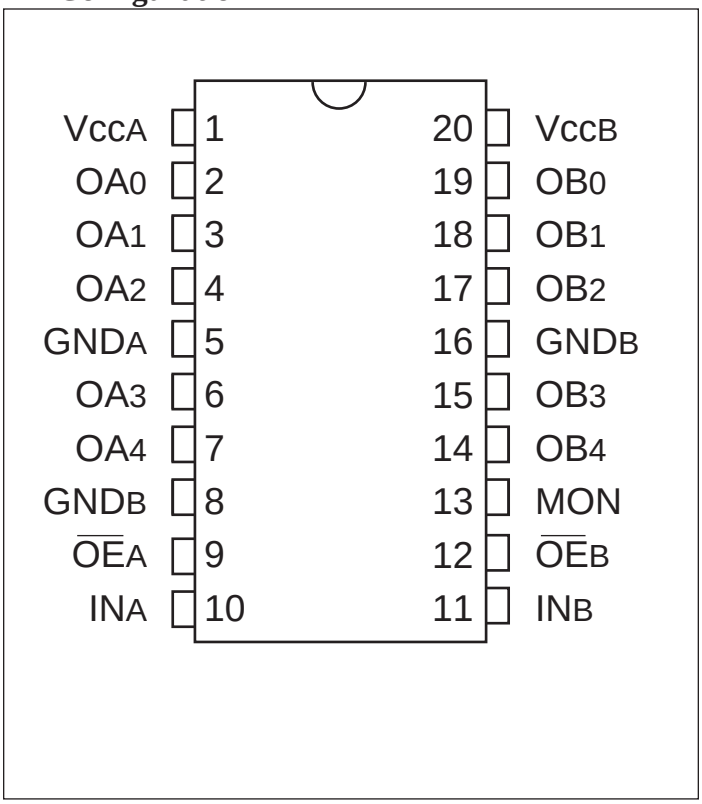
Pericom Semiconductor's PI49FCT805T and PI49FCT2805T are non-inverting clock drivers. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL-compatible CMOS input.

The PI49FCT2805T features a 25-ohm on-chip resistor for lower noise.

Block Diagram



Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = –40°C to +85°C, VCC = 5.0V ± 5%)

rameters	Description	Test Conditions(1)		Min.	Typ(2)	Max.	Units
Voh	Output HIGH Voltage	Vcc = Min., Vin = Vih or Vil	Ioh = –24.0mA	2.4	3.3		V
Vol	Output LOW Current	Vcc = Min., Vin = Vih or Vil	Iol = 64mA		0.3	0.55	V
			Iol = 12mA (25W)		0.3	0.50	V
Vih	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
Vil	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
Iih	Input HIGH Current	Vcc = Max.	Vin = Vcc			1	µA
Iil	Input LOW Current	Vcc = Max.	Vin = GND			–1	µA
Iozh	High Impedance	Vcc = Max.	Vout = Vcc			1	µA
Iozl	Output Current		Vout = GND			–1	µA
Ii	Input HIGH Current	Vcc = Max., Vin =Vcc (Max.)				20	µA
Vik	Clamp Diode Voltage	Vcc = Min., Iin = –18mA			–0.7	–1.2	V
Ios	Short Circuit Current	Vcc = Max.(3), Vout = GND		–60	–120	–225	mA
Vh	Input Hysteresis	Vcc = 5 V			200		mV

Capacitance

Parameters	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions		Min	Typ	Max.	Units
Icc	Quiescent Power Supply Current	Vcc = Max.	Vin = GND or Vcc		3	30	µA
DIcc	Supply Current per Input @ TTL HIGH	Vcc = Max.	Vin = 3.4V(3)		0.5	2.0	mA
Iccd	Supply Current per Input per MHz(4)	Vcc = Max., Outputs Open, OEa = OEb = GND, Per Output Toggling, 50% Duty Cycle	Vin = Vcc, Vin = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current	Vcc = Max., Outputs Open f_I = 10MHz 50% Duty Cycle OEA = OEB = GND	Vin = Vcc, Vin = GND		7.7	14.0[5]	mA
					8.0	15.0[5]	
		Five Outputs Toggling Vcc = Max., Outputs Open f_I = 10MHz 50% Duty Cycle OEA = OEB = GND	Vin = 3.4V, Vin = GND		4.3	8.4[5]	
					4.8	10.4[5]	

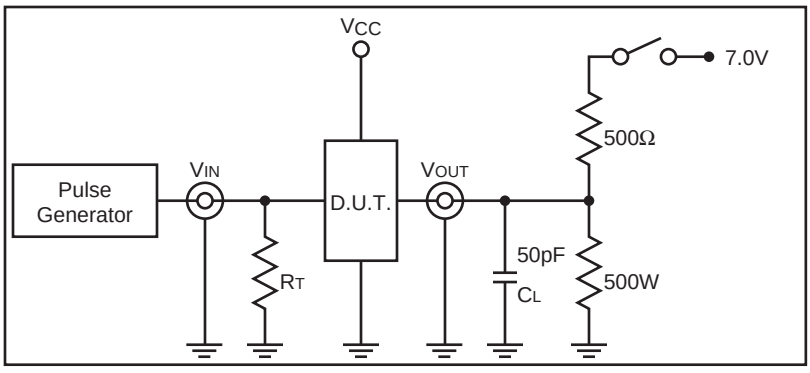
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (Vin = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. Ic =Iquiescent + Iinputs + Idynamic
   Ic = Icc + DIcc DhNt + Iccd (fcp/2 + fiNi)
   Icc = Quiescent Current
   DIcc = Power Supply Current for a TTL High Input (Vin = 3.4V)
   Dh = Duty Cycle for TTL Inputs High
   Nt = Number of TTL Inputs at Dh
   Iccd = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fcp = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   fi = Input Frequency
   Ni = Number of Inputs at fi
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions(1)	805T/2805T Com. Min.	805T/2805T Com. Max.	805AT/2805AT Com Min.	805AT/2805AT Com Max.	805BT/2805BT Com. Min.	805BT/2805BT Com. Max.	805CT/2805CT Com Min.	805CT/2805CT Com Max.	Units
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_N, IN_B to OB_N	CL = 50pF RL = 500Ω	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_A$ to $\overline{OA}_N$, $\overline{OE}_B$ to $\overline{OB}_N$		1.5	8.0	1.5	8.0	1.5	8.5	1.5	6.2	
t_{PHZ} t_{PLZ}	Output Disable Time(4) $\overline{OE}_A$ to $\overline{OA}_N$, $\overline{OE}_B$ to $\overline{OB}_N$		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	
$t_{SKEW(o)}$(3)	Skew twx two outputs of same package (same transition)		—	0.7	—	0.5	—	0.4	—	0.4	
$t_{SKEW(p)}$(3)	Skew twx opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	0.7	—	0.5	—	0.5	
$t_{SKEW(t)}$(3)	Skew twx two outputs of different package at same temperature (same transition)		—	1.5	—	1.0	—	1.0	—	1.0	

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. This parameter is guaranteed but not production tested.

Tests Circuits For All Outputs(1)



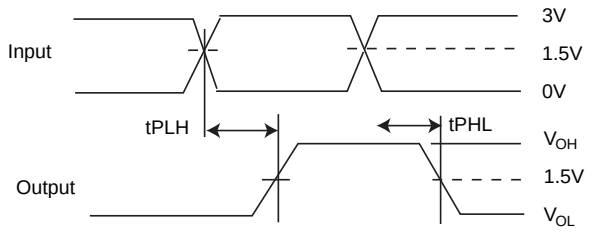
Switch Position

Test	Switch
Open Drain Enable LOW Disable LOW	Closed
All other inputs	Open

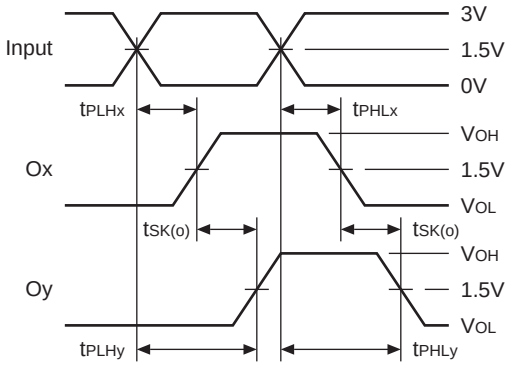
Definitions:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Switching Waveforms

Propagation Delay

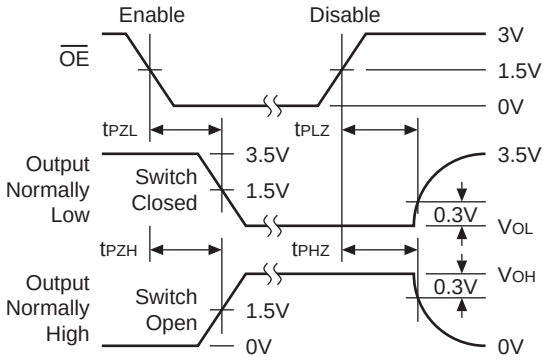


Output Skew – tsk(o)

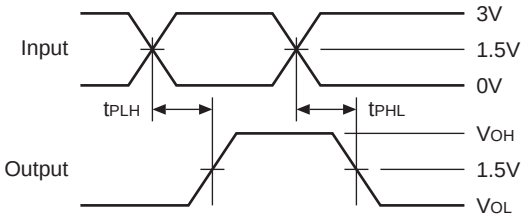


$t_{SK(o)} = | t_{PLHy} - t_{PLHx} |$ or $| t_{PHLy} - t_{PHLx} |$

Enable and Disable Times

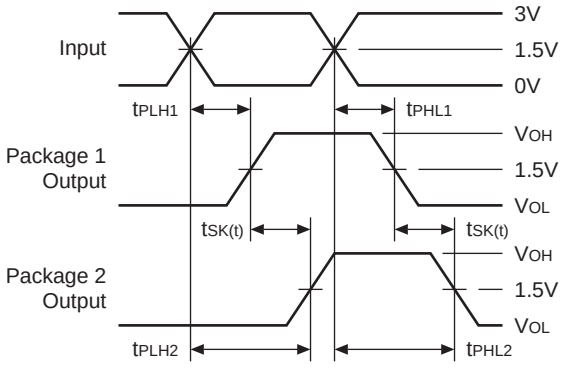


Pulse Skew – tsk(p)



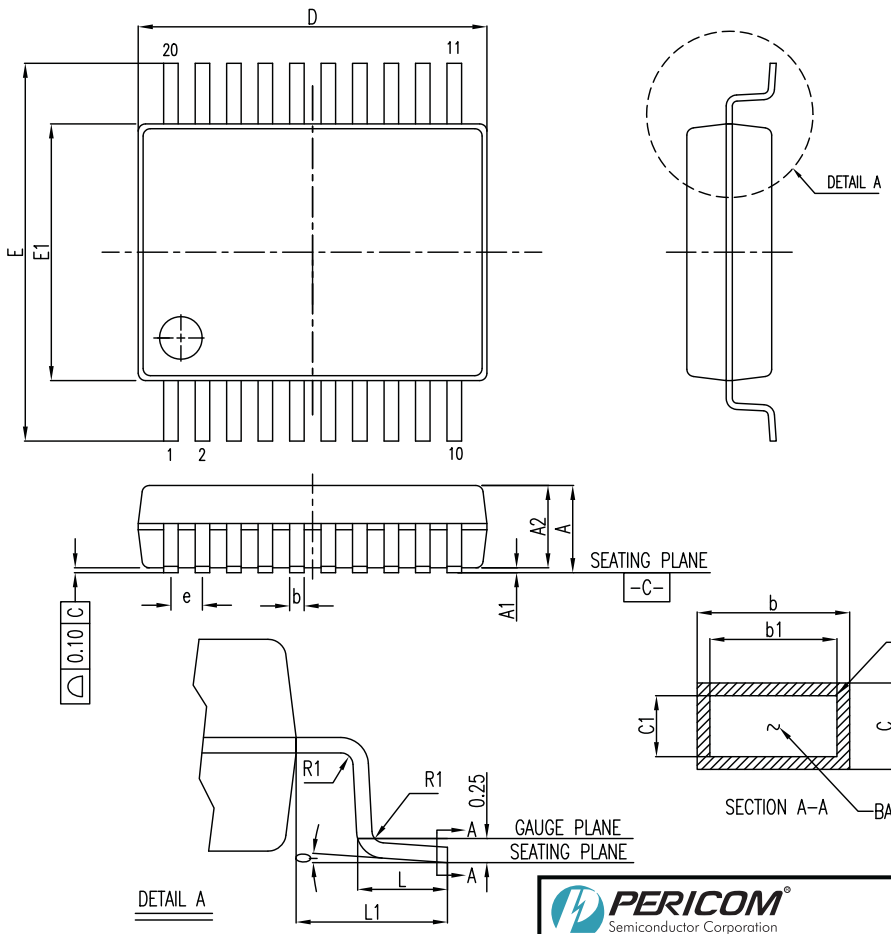
$t_{SK(p)} = | t_{PHL} - t_{PLH} |$

Package Skew – tsk(t)



$t_{SK(t)} = | t_{PLH2} - t_{PLH1} |$ or $| t_{PHL2} - t_{PHL1} |$

Packaging Mechanical: 20-Pin 209-Mil SSOP (H)



SYMBOL	COMMON DIMENSION MILLIMETERS		
	MIN.	NOM.	MAX.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
b1	0.22	0.30	0.33
c	0.09	--	0.25
c1	0.09	0.15	0.21
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
D	6.90	7.20	7.50
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF.		
R1	0.09	--	--
θ	0°	4°	8°

NOTE:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-150B/AE
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM Semiconductor Corporation

DATE: 04/10/08

DESCRIPTION: 20-Pin, 209-Mil Wide, SSOP

PACKAGE CODE: H20

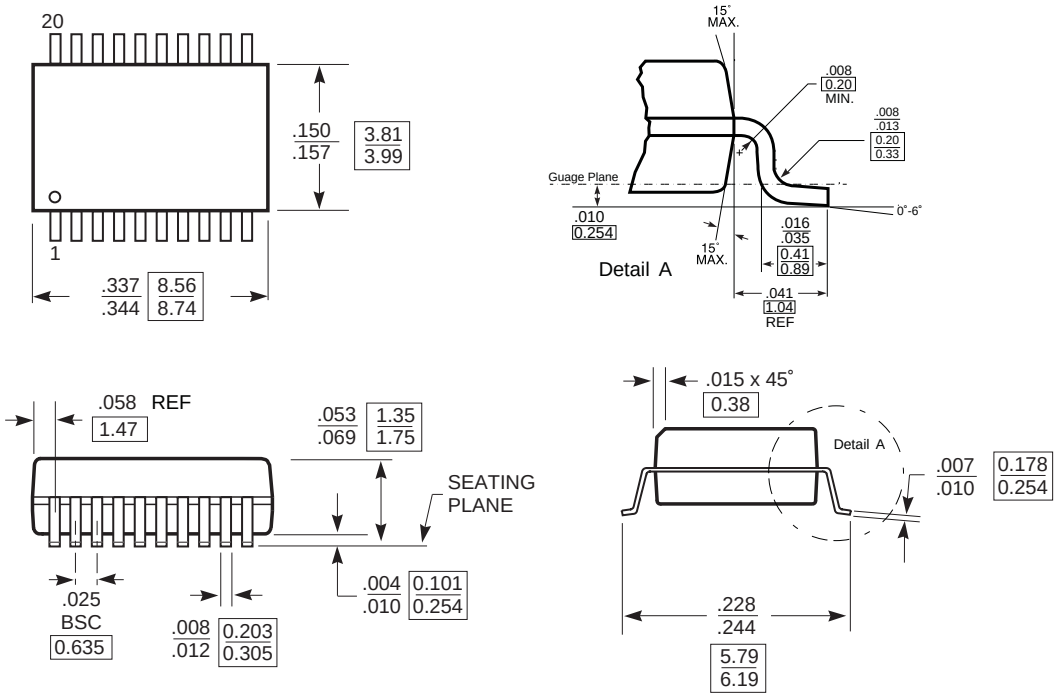
DOCUMENT CONTROL #: PD-1240 **REVISION: E**

08-0140

Packaging Mechanical: 20-Pin 150-Mil QSOP (Q)

DOCUMENT CONTROL NO.
PD - 1202

REVISION: H
DATE: 10/22/07



X.XX / X.XX DENOTES DIMENSIONS IN MILLIMETERS

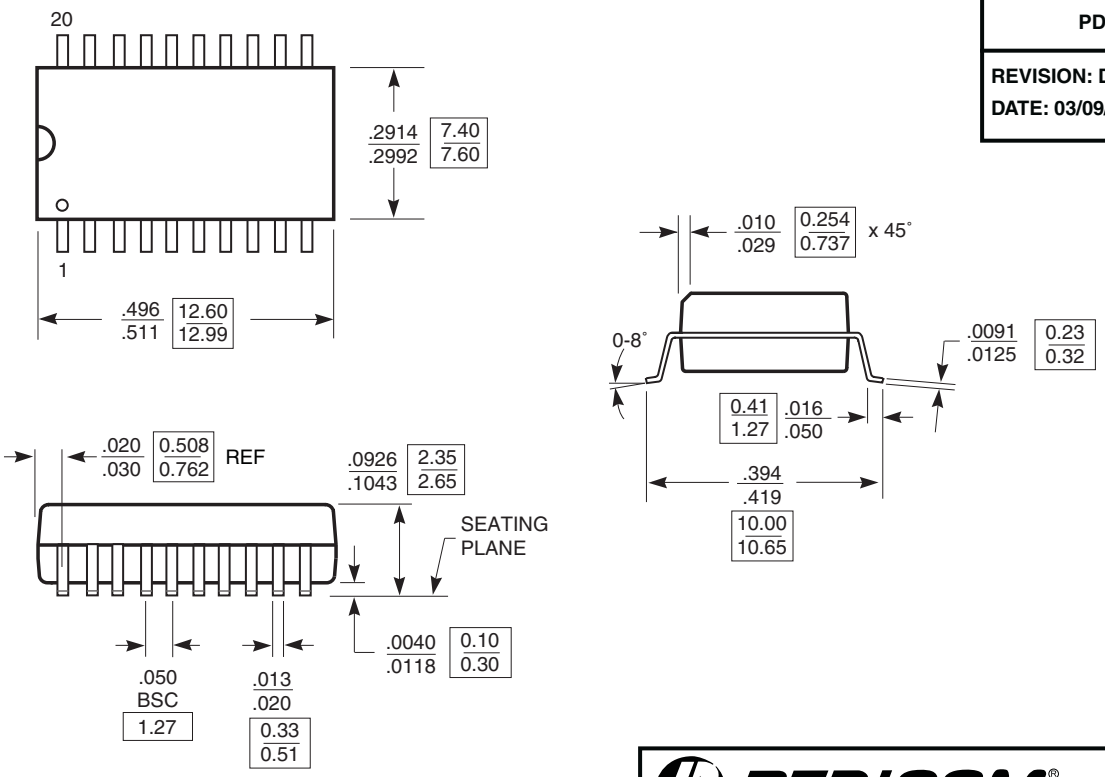
Note:
1) Controlling dimensions in inches.
2) Ref: JEDEC MO-137B/AD
3) Dimensions do not include mold flash, protrusions or gate burrs

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 20-Pin, 150-Mil Wide, QSOP

PACKAGE CODE: Q

Packaging Mechanical: 20-Pin 300-Mil SOIC (S)



Notes:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MS-013D/AC

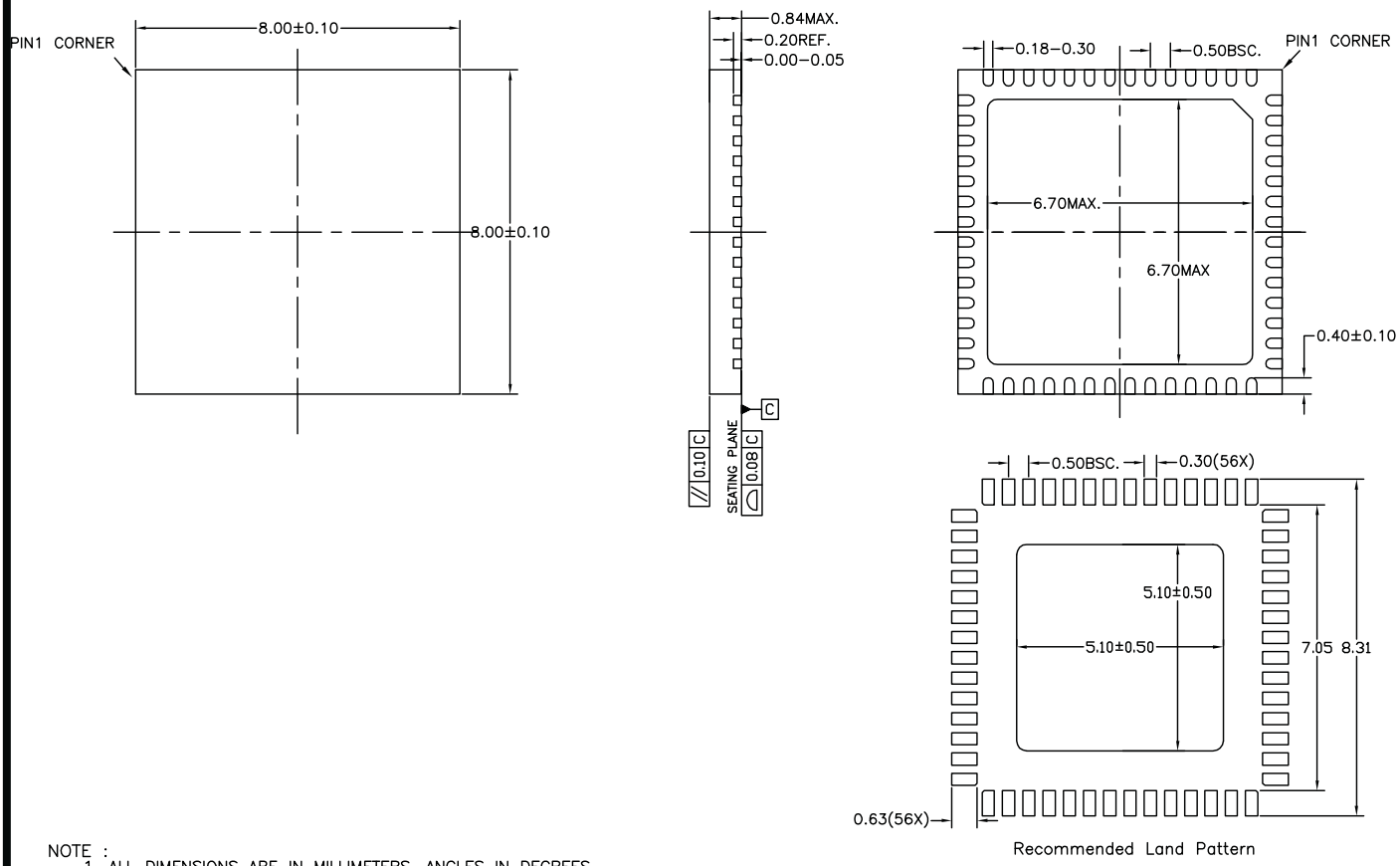
DOCUMENT CONTROL NO.
PD - 1006

REVISION: D
DATE: 03/09/05

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 20-Pin, 300-Mil Wide, SOIC

PACKAGE CODE: S



NOTE :
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES IN DEGREES.
2. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220 MODIFIED.
4. Thermal Via Diameter. Recommended 0.2~0.33mm
5. Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation

DATE: 10/15/08

DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)

PACKAGE CODE: ZB56

DOCUMENT CONTROL #: PD-2008 **REVISION: D**

Ordering Information(1-3)

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT805TSE	S	Blank	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805TH	H	Blank	20-pin 209-mil SOIC
PI49FCT805THE	H	Blank	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805TQE	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805ATSE	S	A	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805ATHE	H	A	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805ATQE	Q	A	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805BTH	H	B	20-pin 209-mil SOIC
PI49FCT805BTHE	H	B	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805BTQE	Q	B	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT805CTS	S	C	20pin 300-mil SOIC
PI49FCT805CTSE	S	C	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT805CTHE	H	C	Pb-free & Green, 20-pin 209-mil SOIC
PI49FCT805CTQE	Q	C	Pb-free & Green, 20-pin 150-mil QSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

Ordering Information for PI49FCT2805T

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT2805TSE	S	Blank	Pb-free & Green, 20pin 300-mil SOIC
PI49FCT2805TQ	Q	Blank	20-pin 150-mil QSOP
PI49FCT2805TQE	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT2805ATQE	Q	A	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT2805BTQE	Q	B	Pb-free & Green, 20-pin 150-mil QSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel